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THE EFFECTS OF INTRINSIC SILICON EPITAXIAL LAYER IN P-I-N DIODE FOR HIGH POWER DEVICES

Cheh Chai Mee[1], M. K. Md Arshad[1, 2], M. F. M. Fathil[1] and U. Hashim[1, 2]
[1]Institute of Nano Electronic Engineering, Universiti Malaysia Perlis, Perlis, Malaysia
[2]School of Microelectronic Engineering, Universiti Malaysia Perlis, Perlis, Malaysia
E-Mail: mohd.khairuddin@unimap.edu.my

ABSTRACT

The p-i-n diode is one of the earliest semiconductor devices developed for power circuit application. The diode is formed with the intrinsically doped i.e. i-layer sandwiched between the p-type and n- type layers. In this paper, we focus on the variables in the intrinsic region of silicon p-i-n diode to the current-voltage characteristics. In our structure, n-type refers to the bulk substrate and intrinsic region refers to the epitaxial layer of the silicon substrate. Result shows that intrinsic layer optimization has successfully enhanced the diode device robustness in terms of diode current-voltage characteristics, which reflects better manufacturing yield and improve the final product performance.

Keywords: power devices, p-i-n diode, epitaxial layer.

INTRODUCTION

A material that has an ability to conduct electric current in between conductors and insulators is known as semiconductor (Floyd, 2008). In semiconductor technologies, a diode is formed when a piece of intrinsic silicon is doped with n-type dopant and another part is doped with p-type dopant. A p-n junction will be formed at the boundary between these two regions (Baliga, 1996). An evolution of p-n diode happened when there is an extra intrinsic layer formed between p-type and n-type dopants. The p-i-n rectifier is one of the very first semiconductor device developed for power circuit applications (Baliga, 1996). Figure-1 illustrates the p-i-n diode structure.

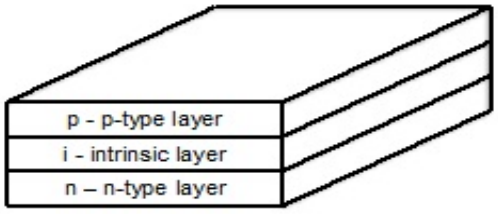

Figure-1. 2D structural layer P-i-N diode.

P represents the p-type layer, n represents the n-type layer, i represents the intrinsic layer that stack in between p-type and n-type layer. The intrinsic layer makes this diode ideal for fast switches. Another unique characteristic for p-i-n diode is its low voltage drop and high breakdown voltage. The width of the low-doped base region, define the reverse breakdown of the p-i-n diode. Basically, p-i-n diode widely used in power electronic applications as their central layer can withstand high voltages. There are quite a number of studies for the past decades to explain the behavior of small-signal low power p-n junction diodes (Baliga, 1987; Gandhi, 1977; Hall, 1952; Jubadi & Noor, 2010; Kingston, 1954; Mazhari, Sinha, & Dixit, 2006; Moll, 1964; Pendharkar, Trivedi, & Shenai, 1996; Salah *et al.* 2007; Sze, 1969; Tsukuda, Sakiyama, Ninomiya, & Yamaguchi, 2009) and high-power p-i-n diode (Abiri, Salehi, Kohan, & Mirzazadeh, 2010; Jablonski, 1998; Sawant & Baliga, 1999; Shuhaimi *et al.* 2010).

In this study, a commercially available 600 V p-i-n diode was used to investigate the effects of changes in i-region width on the current-voltage (I-V) performances. Basically, the main yield loss of this device is related to low reverse breakdown and high reverse leakage. Low yield is not only related to reduce of profit margin, but also caused the diode not robust for power device. Since p-i-n diode operates in a thickness-limited mode, which is controlled by the width of an i-region, the factors need to be taken into consideration is the epitaxial specification which includes epitaxial thickness and epitaxial resistivity. The given specification for epitaxial thickness is from 89 - 102.7μm with resistivity ranges from 30 – 42 Ωcm. High epitaxial thickness which will lead to high reverse voltage (VR) and high forward voltage (VF) since VR is proportional to VF. The relationship for reverse voltage, forward voltage and reverse leakage can be shown as in Equation (1), where VF= Forward Voltage, VR= Reverse Voltage, IR= Reverse Leakage.

$$VF = VR, VR = \frac{1}{IR} \quad (1)$$

VF = Forward Voltage,
VR = Reverse Voltage,
IR = Reverse Leakage

This p-i-n diode has a relatively small operating margin for forward and reverse breakdown voltage. Despite that, there are a few factors that should be taken into consideration for improving the device yield and performance, which should reflect to robustness of production variation.

The first approach is to adjust the depth of the p-junction through boron diffusion. By reducing the junction diffusion drive time, a shallower p-junction is formed and

giving a higher reverse breakdown and lower reverse leakage (IR). However, this method is less favorable due to the drawbacks as stated here:

- There is a process variation for p- junction diffusion depth from time to time. Process variation is unavoidable in mass production. This is due to the furnace that cannot produce constant result of junction depth throughout all the time.
- Furnace to furnace variation will be an additional factor in controlling of the electrical parameter. As the p-junction diffusion is done at a high temperature, there will be a significant amount of up diffusion from the heavily doped bulk substrate. Adjusting p-junction drive in recipe may not be a wise idea due to the uncontrollable nature of the bulk dopant up diffusion from bulk substrate resulting in variation of the final profile of the epitaxial layer, translating to the breakdown voltage. Up diffusion refers to the diffusion rate from bulk substrate (n- type layer) to intrinsic layer during p- type dopant diffusion. If there is a high variation in any of the processes, it may lead to high reverse breakdown and high forward voltage as the reverse breakdown is proportional to forward voltage. High forward voltage will create another yield loss issue and hence boron diffusion adjustment is not a good idea to solve the yield issue.

Second approach is to adjust the epitaxial layer profile of the substrate. Epitaxial layer refers to the intrinsic layer in the p-i-n diode. Thicker epitaxial layer will lead to higher reverse breakdown, while thin epitaxial layer will lead to lower reverse breakdown. This is because the diode funtions in the punch-through operation mode. In this paper we will discuss on how effective this approach to fix the poor electrical performance and electrical over stress (EOS) of the p-i-n 600 V diode. This is more favorable as there will be no process-to-process variation during fabrication process and it is more controllable.

The p-i-n diode is operating in epitaxial limited mode. From semiconductor physics theory, the breakdown voltage is controlled by the thickness of the n- epitaxial layer that remains after all the high cycle thermal fabrication process. The profile of the current epitaxial is shown in Figure-2, which the p-i-n diode is constituted of the bulk and the silicon epitaxial layer. The bulk has a very low resistivity (1.1 mΩ.cm to 1.9 mΩ.cm) compare to the epitaxial resistivity, which has a higher resistivity (30 to 42 Ω.cm). By adjusting epitaxial thickness and epitaxial resistivity, we can target the desired breakdown and hence the high reverse leakage issue can be solved due to reverse breakdown voltage is inversely proportional with reverse leakage current i.e. high reverse breakdown will lead to low leakage.

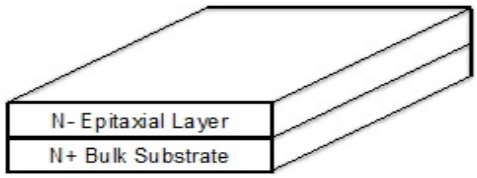

Figure-2. Current epitaxial profile.

METHODOLOGY

Methodology in this work includes fabrication of p-i-n diode and measurement of current-voltage characteristic at wafer level. In the device specification, there is a certain requirement (i.e. thickness and resistivity) of epitaxial layer in order to achieve a specific range of reverse breakdown as shown in Table-1.

Table-1. Specification limit for substrate of the investigated diode.

Specification	Thickness [µm]	Resistivity [Ω.cm]
Existing specification	89.3 – 102.7	30.02 – 42.66

Firstly, we design four corners matrix Design of Experiment (DOE) with three variables, which include epitaxial thickness, epitaxial resistivity and boron dopant junction drive time as detailed-out in Table 2. The four corners matrix is groups of epitaxial layer that covers the lower and upper specification as illustrated in Figure 3. Four corners matrix is used in this evaluation to study the p-i-n diode performance when operating at the corner (lower or upper end) of epitaxial specification compared with center. The p-i-n diode (wafers) are then fabricated and bring to wafer level testing which is also known as probing by using tester. Electrical data obtained from probing is then analyzed using commercial statistical software. Using statistical software, the profiler study was done to determine the dominant factor that impacts the part electrical performance and the optimal epitaxial profile. Wafer from each of the DOE splits is then sent for assembly test to get the final electrical data. The finished units were then submitted for characterization and Unclamped Inductive Surge testing (UIS) as final confirmation. The UIS test is a maximum peak current a diode can sustain before failure.

The acronym C (Table-2 and Figure-3) refers to the center group, H refers to the high group and L refers to the low group. In this case, we have taken into consideration, the impact at the four corners area in the device specification. We use three variables which include epitaxial thickness, epitaxial thickness and boron drive time to form a DOE matrix. From three variables and four corners (C, H, L) we can have twelve splits design of evaluation. For comparison purpose, the device is also fabricated with center of thickness, resistivity and boron drive time as a control wafer.

From all the results, a proposed new epitaxial window specification will be derived. To ensure the repeatability of the result, process is repeated for wafer fabrication up to wafer level testing. This helps to ensure the new epitaxial window specification fit the 600 V p-i-n diode performances.

Table-2. The DOE matrix for substrate evaluation.

Epitaxial Thickness [µm]	Epitaxial Resistivity [Ω.cm]	Boron Drive Time
L	L	L
L	L	C
L	H	L
L	H	C
C	C	L
C	C	C
C	C	H
H	L	C
H	L	H
H	H	C
H	H	H
Control	Control	Control

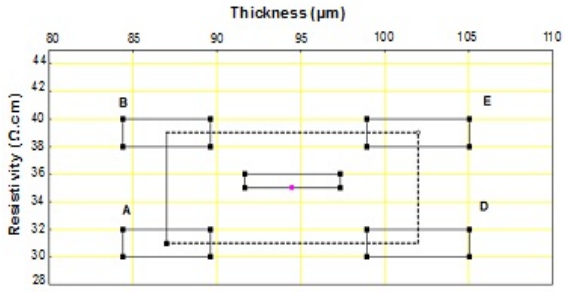

Figure-3. The location of four corner samples.

RESULTS AND DISCUSSIONS

Figure-4 shows the contour profile of the four corner DOE evaluation with resistivity as a function of thickness. The color represents the characteristics for the given epitaxial thickness and resistivity. The main interested area in the profile is white zone since this is the best zone condition to achieve a robust device, which mean other colors (i.e. red, green, blue, light chocolate and purple) are not important, which can be ignored in the analysis. We test the electrical parameter in accordance of diode performance. Red color represents forward voltage (VF) parameter tested at 3 V. Blue color represents reverse breakdown (VR) testing at 100 µA. Green color represents reverse (IR1) breakdown testing at 20 µA. Light chocolate color represents reverse leakage (IR2) parameter testing at 615 V. Purple color represents Delta reverse breakdown (DVR) that is used to test the sharpness of the reverse breakdown at different biasing. One can see, red color (VF), the device will fail at the epitaxial thickness of around 99 µm for all the resistivity values. At around 90 µm, the part will fail for VR parameter as indicated by blue color profiler. Green (IR1) and light chocolate (IR2) color represents reverse leakage and it shows the device will fail for reverse leakage test at epitaxial thickness of around 92 µm and if the epitaxial resistivity lower than 37.5Ωcm. DVR parameter is the most robust, which no impact by the variation of resistivity and thickness. In order to design a robust p-i-n diode, each electrical parameter of the p-i-n diode needs to take into consideration. This is how the four corners matrix with three variables DOE is developed to evaluate the optimum epitaxial specifications for p-i-n diode. The biasing limit, testing and specification limits were defined in customer datasheet with the key aim to meet all tests within a specification. For examples we have VF@3A, VR@20uA, VR@100uA, IR@3.48uA, IR@5uA and DVR<18V tests. In general, we would like to stress out that, the white region is the optimum window to produce a robust p-i-n diode.

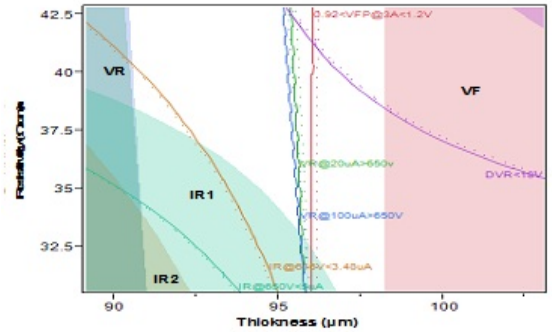

Figure-4. Contour profiler of four corners matrix.

The electrical data collected through probing for each of the DOE splits were then put into statistical prediction profiler software to obtain the most optimum epitaxial window for p-i-n 600 V diode as shown in Figure-5. One can see that (from the desirability curve), the epitaxial thickness is a dominant factor to determine the reverse breakdown and epitaxial resistivity only gives a minor impact (with less variation compared with the impact of thickness) to the device performance. The result indicates p-i-n diode operates fitly in the epitaxial thickness of ~96 µm. The curvature of the line in desirability row indicates how impactful the two factors (epitaxial thickness and epitaxial resistivity) to the electrical parameters of the device. This can be seen when the line for epitaxial thickness is in responsive form compared to the straight line from epitaxial resistivity. Prediction profiler also shows the desirable epitaxial layer thickness and epitaxial resistivity to create a robust p-i-n diode. The optimum specification for an epitaxial thickness and resistivity are 96 µm and 36 Ω.cm, which is correspondence with center white zone of Figure-4.

After we obtain the electrical performances, we proceed with high volume fabrication process to determine the production yield. Table-3 shows the total yield from the evaluation split using four corners matrix with three DOE variables (see Table-2). For better visualization of

the table, it is repeated here that, CCL represent the splits is from center epitaxial thickness, center epitaxial resistivity and low boron dopant diffusion time. From the table, some wafers do not have yield due to they were scrapped for wafer breakage during fabrication. There are 12 groups of splits in totals. One can see that, cell with center group of epitaxial thickness and resistivity produces higher yield with above 99 % regardless on boron dopant diffusion times (low, center or high group).

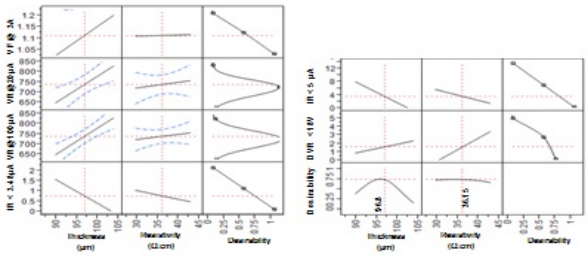

Figure-5. Prediction profiler of 4 corners matrix.

Table-3. The DOE matrix for substrate evaluation.

		Lot 1	Lot 2	Lot 3
Group	Wafer	Yield	Yield	Yield
A. LLL.	10	3.44	11.34	42.42
A. LLL.	11	6.55	3.99	53.70
B. LLC.	9	6.91	2.66	10.52
B. LLC.	12	3.11	0.68	24.52
C. LHL.	14	82.19	50	86.10
C. LHL.	15	54.75	58.45	81.56
D. LHC.	13	82.57	53.76	83.38
D. LHC.	16	25.64	35.34	92.37
E. CCL.	3	99.98	-	99.87
E. CCL.	8	99.43	100	99.92
F. CCC.	4	-	99.32	99.89
F. CCC.	6	99.79	100	99.87
G. CCH.	5	97.02	99.32	99.03
G. CCH.	7	99.96	100	99.85
H. HLC.	17	46.13	78.54	28.33
H. HLC.	20	57.41	73.19	19.39
I. HLH.	18	45.75	30.67	32.07
I. HLH.	19	63.05	80.54	50.97
J. HHC.	21	58.47	38	16.05
J. HHC.	24	84.18	39.33	40.98
K. HHH.	22	76.68	32	37.07
K. HHH.	23	85.02	56.63	8.41
L. Control.	1	100	99.32	99.81
L. Control.	2	99.92	100	99.92

The cells are then proceeds with wafer characterization and followed by unclamp inductive surge test (UIS) to evaluate the robustness of the device using new substrate epitaxial. UIS test is to determine a maximum peak current for a diode can sustain before failures. Figure-6 shows the UIS result analyzed using statistical prediction profiler for certain cell (representing higher, average and lower production yield – see Table-3) on the impact of epitaxial thickness, epitaxial resistivity and boron drive time for three different lots. It shows that, low epitaxial thickness results in higher mean energy, high epitaxial thickness has lower mean energy and center matrix of epitaxial thickness has the mean energy in between. The result shows similarity for three different lots, to show good repeatability is obtained. This analysis is further validate the result in Figure-5 i.e. epitaxial resistivity has more dominant impact. In this case, to achieve a good UIS performance, epitaxial thickness plays a dominant factor compared than that of epitaxial resistivity and boron diffusion as shown in Figure-7. This is because the main electrical parameter show more responsive curve to epitaxial thickness compared to epitaxial resistivity and boron drive time. The main parameters to be taking care is the forward voltage (VF), reverse breakdown (VR), Reverse current (IR) and also the energy. From the prediction profiler, again it shows that epitaxial thickness plays a huge impact to all the four parameters as the epitaxial thickness line is more responsive compare to other two variables. In addition to that, although low epitaxial thickness results in highest energy, but this group has high electrical failure rate (see Table-3), thus in this case CCC group is better choice since it has acceptable range energy level with highest yield.

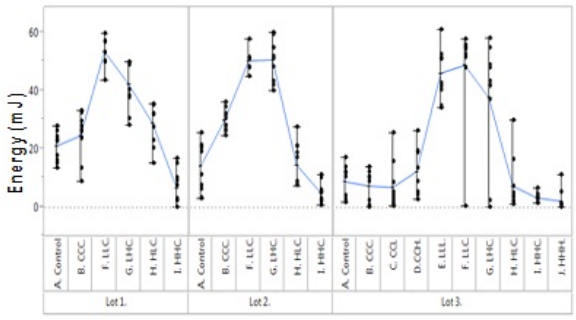

Figure-6. Contour profiler of four corners matrix.

Figure-8 shows the electrical parameter and distribution for each of the cells from DOE. Figure 8 (a) shows the forward voltage testing at 3 A. One can see that, three different levels i.e. high, middle and low VF is achieved in middle and low group, but the population results are still within upper and lower specification. High VF produces a bit high, and almost out limit (at 1.2 V) of upper VF specification. High, low and middle VF are from high, low and middle thickness of epitaxial layer respectively. We can see that epitaxial resistivity and boron diffusion does not influence the VF parameters compare to epitaxial thickness. This can be observed where the cell CCL, CCC and CCH have the same trend for VF (middle). The same trends also go to center matrix cell LLL, LLC, LHL and LHC, which yield lowest VF. Lastly for high VF group cell, it occurs for specification with HLC, HLL, HHC and HHH. Figure-8 (b) shows the reverse breakdown (VR) at 20 μA, tested at 615 V. Similar trend as previous seen on VF can be observed. Figure-8 (c) shows the leakage test (IR) for the p-i-n diode. The limit is 3.48 uA respectively. The cells from low epitaxial

thickness matrix have wide spread and fail for reverse leakage test. We can then conclude cell from low epitaxial thickness matrix are not fit for 600 V p-i-n diode. Cell from high matrix have lower leakage due to the higher reverse breakdown, lower reverse leakage. Overall cells from center and cell from the high group pass the reverse leakage limit. Figure-8 (d) represents the Delta reverse breakdown (DVR) of each of the cells. Delta reverse breakdown to test the sharpness of the reverse breakdown at different biasing at 20 µA and 100 µA. From the figure, all cells have comparable delta reverse breakdown trend except for cells from high groups have poorer delta reverse breakdown.

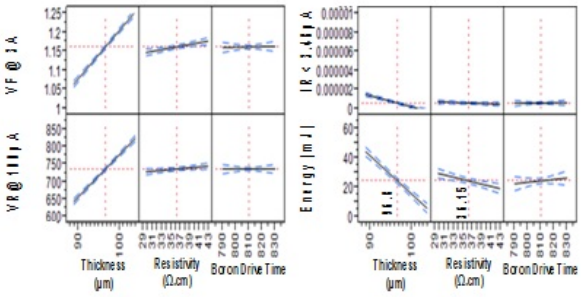

Figure-7. Prediction profiler of four corners matrix.

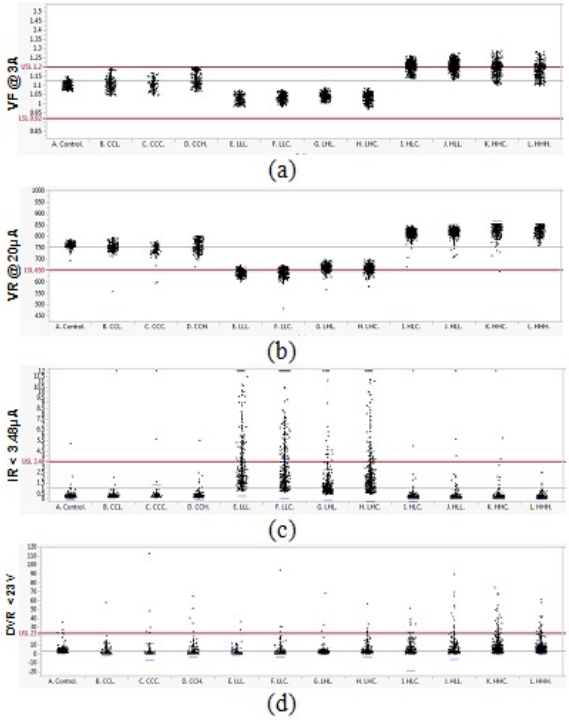

Figure-8. The electrical parameter and distribution for each of the cells from DOE. (a) The VF distributions for all the cells at 3A biasing testing. (b) The VR distributions for all the cells at 20 µA biasing testing. (c) The IR leakage test distributions for all the cells at 3.48 A limit. (d) The Delta VR testing distribution for all the cells between two biasing, 20 µA and 100 µA.

Figure-8 is the electrical distribution for all the test parameters obtained from four corner matrix splits. It shows low group and high group (especially epitaxial thickness) will fail certain electrical parameter in the given specification for diode. For example, low matrix will bring yield loss in terms of high reverse leakage (IR) and low reverse breakdown (VR). High matrix will bring yield loss in terms of high forward voltage (VF).

Figure-9 shows the overall energy contour plot versus epitaxial thickness and epitaxial resistivity. Based color contour, the p-i-n diode will have better energy at lower epitaxial thickness. Blue color indicates high energy and red color represents low energy. This shows that, the lower the epitaxial thickness, the higher the energy and vice versa. As epitaxial thickness higher, the energy is lower which is not desirable for a p-i-n diode. Lower epitaxial thickness will lead to lower reverse breakdown and higher reverse leakage, which is not desirable for p-i-n diode. In order to find a balance between both energy level and also electrical parameter, 96 µm of the epitaxial thickness is the optimum window to produce a robust device that fit the electrical parameter and withstand high energy.

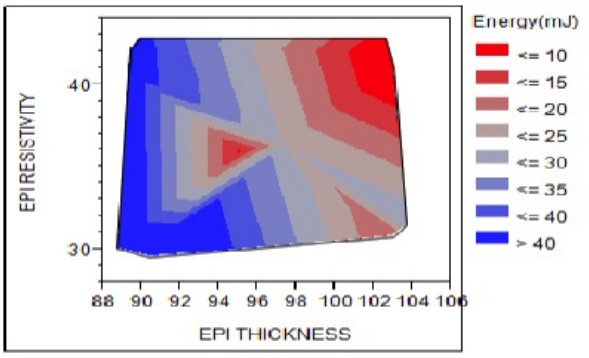

Figure-9. Contour plot for energy of UIS.

With the implementation of new epitaxial specification into production line, the p-i-n medium voltage diode has increased in yield from 84 % to 97.4 % through the year of 2013 to 2014. Figure-10 shows the medium voltage yield trend the yield start to stabilize after new epitaxial implementation.

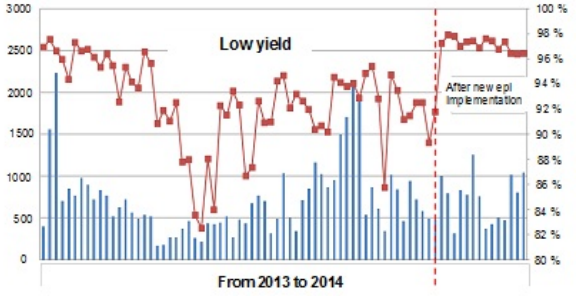

Figure-10. p-i-n diode yield trend.

CONCLUSIONS

In summary, through the understanding of the device behavior and by applying a systematic approach to optimize the epitaxial, we have improved the device robustness in terms of electrical performance. The investigation was based on three factors DOE splits for epitaxial thickness, epitaxial resistivity and boron junction depth formation recipe. A statistical analysis based on the electrical data was then carried out to determine the best window for substrate. The parts were then assembled and undergo reliability and characterization test to ensure it meets customer application and pass UIS test. From the evaluation we can conclude that the best window for substrate is at 91 - 99 um for epitaxial thickness, 31-39 ohm.cm for epitaxial resistivity. The implementations of the new epitaxial specification have successfully improved the device robustness.

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